D FLIPFLOP

module dff\_sync\_reset (data , clk , reset , q);

input data, clk, reset ;

output q;

reg q;

always @ ( posedge clk)

if (reset)

begin

q <= 1'b0;

end

else

begin

q <= data;

end

endmodule

TESTBENCH

module dff\_reset\_tb;

reg data, clk, reset ;

wire q;

dff\_reset dffr (.data(data), .clk(clk), .reset(reset) ,.q(q));

initial

begin

clk=0;

data = 0;

reset = 1;

#5 reset = 0;

#80 reset = 1;

$monitor($time, "\tclk=%b\t ,reset=%b\t, data=%b\t, q=%b",clk,reset,data,q);

#100 $finish;

end

initial

begin

$dumpfile("dump.vcd");

$dumpvars(1);

#10000$finish;

end

always

#5 clk = ~clk;

always

#30 data = ~data;

endmodule